

**Claim Amendments:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor processing component comprising SiC, wherein an outer surface portion of the component (i) consists essentially of CVD-SiC, and (ii) has a surface impurity level that is not greater than  $[[10]]5$  times a bulk impurity level.
2. (Original) The component of claim 1, wherein the bulk impurity level is measured at a depth of at least 3  $\mu\text{m}$  from an outer surface of the outer surface portion.
3. (Canceled)
4. (Currently Amended) The component of claim  $[[3]]1$ , wherein the outer surface portion is a CVD-SiC layer deposited over a substrate.
5. (Original) The component of claim 4, wherein the substrate comprises SiC.
6. (Original) The component of claim 5, wherein the substrate comprises SiC impregnated with elemental silicon.
7. (Original) The component of claim 6, wherein the substrate comprises recrystallized SiC impregnated with elemental silicon.
8. (Original) The component of claim 4, wherein the CVD-SiC layer has a thickness within a range of about 10 to about 1000  $\mu\text{m}$ .
9. (Original) The component of claim 4, wherein the CVD-SiC layer has a thickness within a range of about 10 to about 800  $\mu\text{m}$ .

10. (Currently Amended) The component of claim [[3]]1, wherein the component is a free-standing CVD-SiC component.

11. (Original) The component of claim 10, wherein the component consists essentially of CVD-SiC.

12. (Canceled)

13. (Original) The component of claim 1, wherein the surface impurity level is not greater than 2 times the bulk impurity level.

14. (Original) The component of claim 1, wherein the surface impurity level is not greater than the bulk impurity level.

15. (Original) The component of claim 1, wherein the surface impurity and bulk impurity levels are based on at least one of Cr, Fe, Cu, Ni Al, Ca, Na, Zn, and Ti concentrations

16. (Original) The component of claim 15, wherein the surface impurity and bulk impurity levels are based on at least one of Cr and Fe concentrations.

17. (Original) The component of claim 16, wherein the surface impurity and bulk impurity levels are based on Fe concentration.

18. (Original) The component of claim 16, wherein the bulk impurity level is not greater than  $1E17$  atoms/cc Fe and not greater than  $1E15$  atoms/cc Cr.

19. (Original) The component of claim 1, wherein the semiconductor processing component comprises a component from the group consisting of semiconductor wafer paddles, process tubes, wafer boats, liners, pedestals, long boats, cantilever rods, wafer carriers, process chambers, dummy wafers, wafer susceptors, focus rings, suspension rings.

20. (Original) The component of claim 19, wherein the component is a wafer boat.

21. (Original) The component of claim 1, wherein the component is machined prior to treatment to provide said surface impurity level.

22. – 53. (Canceled)